# HCAL serial link architecture

**Private system servers** (PVSS systems)

HV | LV power supplies | RBXs | Source | Laser | HCAL host

**User PCs** (PVSS Uis)

**Counting room**

Industrial hub RS/Ethernet

Optical insulation?

RS422

**Clock generator**

200m

**Detector periphery**

DC/DC or rectifier

Voltage regulator

**Hub-18 RS/RS**

FPGA

Out  In  Clock  Power

**18 channels**

Out  In  Clock  Power

20m

**Detector inner part**

RS422, RS485?

MM

**RBX**

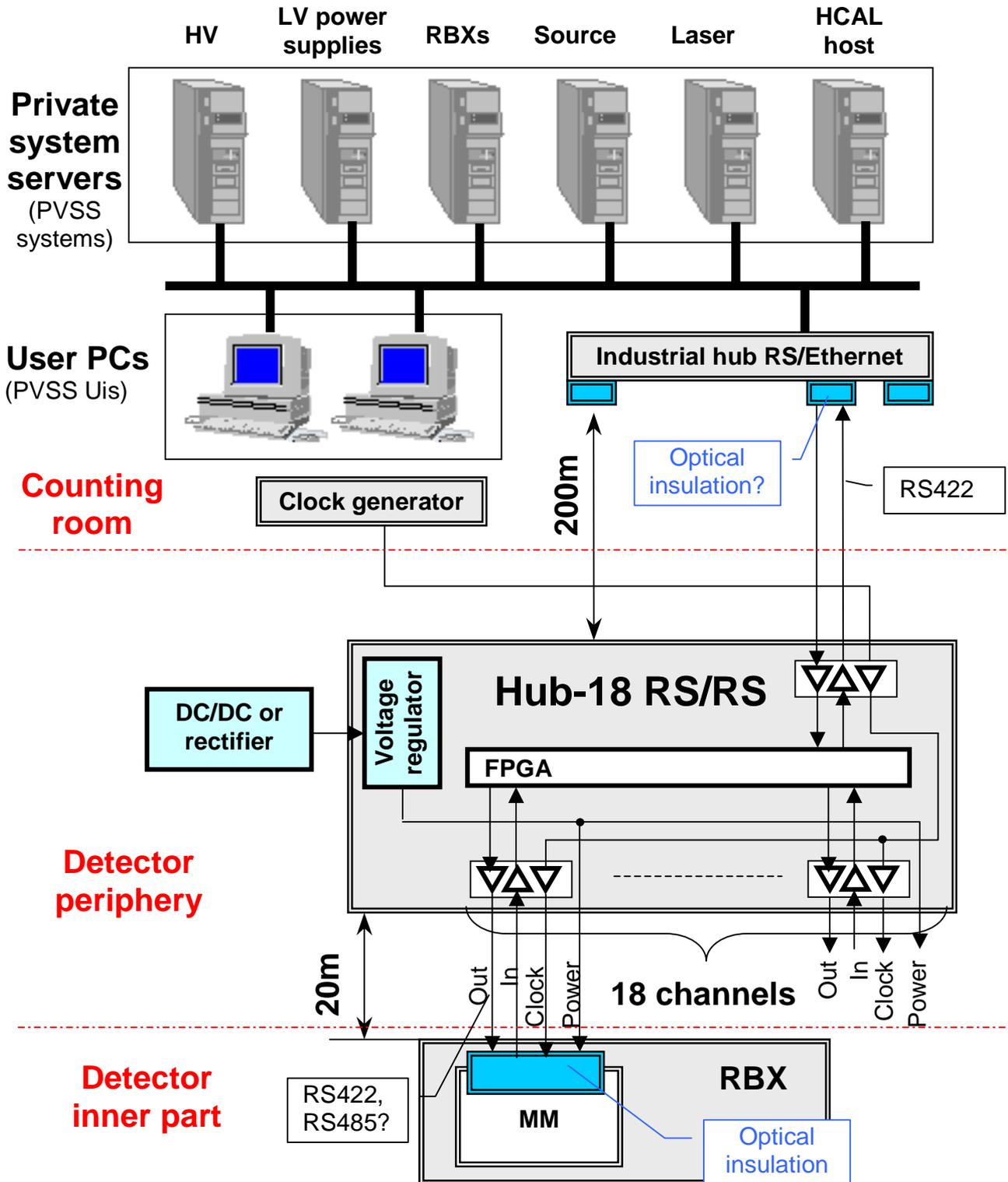Optical insulation

# EMU on-board LV monitoring

EMU electronics scheme is taken from the report of T.Y.Ling at USCMS EMU Meeting Fermilab, October 5-6, 200 (http://cmssun1.ucr.edu:8080/~cms/oct01/oct01.html) see http://www.physics.ohio-state.edu/~ling/elec/emu_elec_status_oct01.pdf

**User interfaces (PVSS)**

**On-board LV monitoring server (PVSS)**

**Ethernet**

**RS/Ethernet hub**

**Cathode LCT - Trig Motherboard**

**DAQ Motherboard**

**Clock Control Board**

**DAQ Interface Board**

*Muon Sector Receiver*
*Lev-1 Trigger*

*(DAQ data)* DDU *SLink* Central Data Acquisition

*Trigger-Timing-Control*

*Slow Control*

*VME Crate*

**RS/RS hub 18**

1 of 1    1 of 5
1 of 5

CFEB CFEB CFEB CFEB CFEB

**Cathode Front-end Board**
3x6 ASICs, 2 FPGAs, channel Links, Buffers

**LV Distribution Board**

LVDB   ALCT   1 of 24

**On-board LV monitoring link**

**Anode LCT Board**
FPGA's, ASICs Channel Links

**Mezzanine board**

CSC

**Anode Front-end Board**
1 ASIC